MicroTESK is a reconfigurable (retargetable and extendable) model-based test program generator for microprocessors and other programmable devices. Lightweight formal specifications customize the generator for a particular architecture and provide knowledge about situations to be covered by tests. A convenient test template framework allows rapid development of complex verification scenarios. Being retargetable, MicroTESK is able to support various RISC and CISC architectures.

Open Source | http://forge.ispras.ru/projects/microtesk

**Microprocessor Specification**
- Specifications in nML/Sim-nML (TU Berlin/IIT Kanpur)
  - memory structure and addressing modes
  - behavioral description of instructions
  - assembler/binary instruction formats
- Configurations in domain specific languages
  - memory management (TLB, L1 and L2)
  - pipeline logic (microarchitectural networks)
  - branch processing (prediction, etc.)

**Target Architectures**
- MicroTESK is retargetable
  - RISC
  - CISC
  - DSP
- Primary focus on RISC architectures
  - ARM
  - MIPS
  - SPARC
  } wide range of ISA
  } + custom designs

**Test Program Generation**
- Test program templates in Ruby
  - focus on simplicity and productivity
  - transparent access to processor model
  - integration with test generators
- MicroTESK is extendable
  - randomized generation
  - combinatorial generation
  } + custom methods

The MicroTESK test program generator is being developed at the Software Engineering Department of the Institute for System Programming, Russian Academy of Sciences (ISPRAS). The institute performs both academic research and industrial development projects as well as provides advanced services and consulting in various areas of software engineering, information technologies and computer science.

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