Verilog Translator - Feature #9990

check for variable/net redeclarations

12/17/2019 05:48 PM - Sergey Smolov

Status:	Closed	**Start date:**	12/17/2019
Priority:	High	**Due date:**	
Assignee:	Alexey Danilov	**% Done:**	50%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Published in build:	0.1.3-beta-201002		

Description

As it is specified in IEEE-1364-2005 Standard for Verilog Hardware Description Language,

```
It is illegal to redeclare a name already declared by a net, parameter, or variable declaration.
```

So the tool should detect erroneous redeclarations.

For more details see 4.2.1 and 4.2.2 chapters.

History

#1 - 02/27/2020 01:22 PM - Sergey Smolov

- Priority changed from Normal to High

- Assignee changed from Alexander Kamkin to Alexey Danilov

- Status changed from New to Feedback

Alexey, could you implement this small feature? It is relevant to your work at VeriTrans.

#2 - 03/03/2020 02:35 PM - Alexey Danilov

- Status changed from Feedback to Resolved

#3 - 03/03/2020 02:36 PM - Alexey Danilov

- % Done changed from 0 to 50

#4 - 03/03/2020 02:40 PM - Alexey Danilov

- Status changed from Resolved to Open

#5 - 04/02/2020 04:24 PM - Alexey Danilov

- Status changed from Open to Resolved

#6 - 04/19/2020 05:34 PM - Sergey Smolov

- Status changed from Resolved to Verified

#7 - 10/02/2020 02:56 PM - Sergey Smolov

- Status changed from Verified to Closed

#8 - 10/02/2020 02:56 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002