Verilog Translator - Bug #9936

tabs in "`define" directive cause java.lang.NumberFormatException

11/20/2019 01:13 PM - Sergey Smolov

Status:	Closed	**Start date:**	11/20/2019
Priority:	High	**Due date:**	
Assignee:	Alexey Danilov	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

Running the **ru.ispras.verilog.parser.VerilogTexas97TestCase#runTest_Pci_Bus_Verilog_Mv_files_PciNorm** test case produces the following error log:

```
ERROR: [Internal] For input string: "    "
java.lang.NumberFormatException: For input string: "    "
    at java.lang.NumberFormatException.forInputString(NumberFormatException.java:65)
    at java.lang.Integer.parseInt(Integer.java:569)
    at java.lang.Integer.parseInt(Integer.java:615)
    at ru.ispras.verilog.parser.model.util.Parser.parseSizeBase(Parser.java:313)
    at ru.ispras.verilog.parser.model.util.Parser.parseNumber(Parser.java:177)
    at ru.ispras.verilog.parser.model.basis.VerilogLiteral.parseNumber(VerilogLiteral.java:46)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_number(VerilogTreeBuilder.java:7636
)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_primary(VerilogTreeBuilder.java:639
0)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_operation(VerilogTreeBuilder.java:6
274)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_expression(VerilogTreeBuilder.java:
6128)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_extended_expression(VerilogTreeBuil
der.java:5403)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_assignment(VerilogTreeBuilder.java:
5333)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_assign_statement(VerilogTreeBuilder
.java:4427)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_statement(VerilogTreeBuilder.java:4
165)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_block_statement(VerilogTreeBuilder.
java:5237)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_statement(VerilogTreeBuilder.java:4
255)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_process(VerilogTreeBuilder.java:330
2)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_item(VerilogTreeBuilder.java:1031)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_module(VerilogTreeBuilder.java:758)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_unit(VerilogTreeBuilder.java:605)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_root(VerilogTreeBuilder.java:553)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.startRule(VerilogTreeBuilder.java:503)
    at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:437)
    at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:442)
    at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:468)
    at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:472)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:193)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.util.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:67)
    at ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_Pci_Bus_Verilog_Mv_files_PciNorm(Ve
rilogTexas97TestCase.java:673)
```

This exception is caused by the line 1045 of *hdl-benchmarks/hdl/texas97/PCI_BUS/Verilog-MV-files/PCInorm.v* file, where tab symbol is used:

```
`define   MemWrite    'h 7
```

History

#1 - 12/03/2019 05:52 PM - Alexey Danilov

- Status changed from New to Resolved

#2 - 12/03/2019 06:15 PM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 10/02/2020 02:56 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed