Verilog Translator - Bug #9915

"Cycle inclusion has been detected in fine <filename>" error is reported for Verilog modules that use the same another file

11/13/2019 03:01 PM - Sergey Smolov

Status:	Closed	**Start date:**	11/13/2019
Priority:	Urgent	**Due date:**	
Assignee:	Alexey Danilov	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

The tool reports "Cycle inclusion has been detected in fine <filename>" error for the case when "a.v" and "b.v" modules include "c.v" module.

To reproduce the bug, checkout to 5ca788cd commit and run **ru.ispras.verilog.parser.VerilogQuipTestCase**. It should be fail-free, but it is not.

IMPORTANT: please run all the project tests before push and compare your results with Jenkins!

History

#1 - 11/14/2019 10:34 AM - Sergey Smolov

IMPORTANT №2: run "./gradlew checkStyle" command in your repo and fix coding style issues in your classes before push too!

#2 - 12/03/2019 02:36 PM - Alexey Danilov

- Status changed from New to Resolved

#3 - 12/03/2019 02:38 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 10/02/2020 02:57 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed