Verilog Translator - Task #9904

add info for "--library-file" cmdline option

11/06/2019 10:38 AM - Sergey Smolov

Status:	Closed	**Start date:**	11/06/2019
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002

Description

Write a description for this option at project wiki.

History

#1 - 11/06/2019 01:44 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 11/06/2019 01:45 PM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 10/02/2020 02:57 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed