Verilog Translator - Task #9899

VerilogPrinter test cases for QUIP benchmarks

10/31/2019 08:53 PM - Sergey Smolov

Status:	Closed	**Start date:**	10/31/2019
Priority:	Normal	**Due date:**	
Assignee:	Maxim Chudnov	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002

Description

History

#1 - 11/12/2019 11:15 AM - Sergey Smolov

- Target version set to 0.1

- Category deleted (Verilog Translator)

- Project changed from Retrascope Test Suite to Verilog Translator

#2 - 11/18/2019 03:31 PM - Maxim Chudnov

- Status changed from New to Resolved

#3 - 11/18/2019 03:33 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 10/02/2020 02:57 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed