Verilog Translator - Bug #9848

ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Pci_Bus_Verilog_Mv_files_PciNorm: Function declaration '$ND' has not been found

10/04/2019 06:24 PM - Sergey Smolov

Status:	Closed	**Start date:**	10/04/2019
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

```
ERROR: Function declaration '$ND' has not been found
ERROR: [Internal] null
java.lang.IllegalArgumentException
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
    at ru.ispras.fortress.util.InvariantChecks.checkFalse(InvariantChecks.java:68)
    at ru.ispras.verilog.parser.VerilogTranslator.exit(VerilogTranslator.java:112)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.checkFunctionCall(Ver
ilogStaticChecker.java:651)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.access$000(VerilogSta
ticChecker.java:72)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker$ExprTreeVisitor.onOpe
rationBegin(VerilogStaticChecker.java:97)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:139)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.checkReference(Verilo
gStaticChecker.java:468)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.checkReference(Verilo
gStaticChecker.java:480)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.checkReference(Verilo
gStaticChecker.java:497)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.checkReference(Verilo
gStaticChecker.java:527)
    at ru.ispras.verilog.parser.backends.syntax.checker.VerilogStaticChecker.onAssignBegin(Verilog
StaticChecker.java:129)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$2.onBegin(VerilogNodeVisitor.java:253)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:700)
    at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:102)
    at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:87)
    at ru.ispras.verilog.parser.VerilogSyntaxBackend.start(VerilogSyntaxBackend.java:80)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:55)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:187)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:72)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:58)
    at ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_Pci_Bus_Verilog_Mv_files_PciNorm(Ve
rilogTexas97TestCase.java:514)
```

History

#1 - 11/02/2019 04:01 PM - Sergey Smolov

It seems to be a dilemma here: either to remove unimplemented function calls from Verilog code or to mark the test case as "should fall".

#2 - 11/05/2019 08:53 PM - Alexander Kamkin

Added --library-file option. See SystfTestCase as an example.

The library file format is as follows: ((function (integer|real)|task) identifier '\n')*.

For example,

```
function integer $myFunction
task $myTask
```

#3 - 11/11/2019 02:01 PM - Sergey Smolov

- % Done changed from 0 to 100

- Assignee changed from Alexander Kamkin to Sergey Smolov

- Status changed from New to Resolved

#4 - 11/11/2019 02:01 PM - Sergey Smolov

- Status changed from Resolved to Verified

#5 - 10/02/2020 02:57 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed