Verilog Translator - Task #9811

macro with parameters

09/05/2019 11:39 AM - Sergey Smolov

Status:	Closed	**Start date:**	09/05/2019
Priority:	High	**Due date:**	
Assignee:	Alexey Danilov	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.2		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002

Description

Macro with parameters are used, for example, in RISC-V cores like picorv32 (see Retrascope for RISC-V).

Related issues:

Related to Retrascope RISC-V Benchmark - Bug #9475: Picorv32Hx8kdemoVerilogPr...	**Closed**	**02/06/2019**
Related to Verilog Translator - Bug #9261: ru.ispras.verilog.parser.Verilogle...	**Closed**	**08/31/2018**

History

#1 - 09/06/2019 02:59 PM - Sergey Smolov

- Related to Bug #9475: Picorv32Hx8kdemoVerilogPrinterTestCase: ERROR: line 1:0 no viable alternative at input '(' added

#2 - 09/06/2019 03:32 PM - Sergey Smolov

- Related to Bug #9261: ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_19_03_01_1: line 1:4 mismatched input ')' expecting LPAREN added

#3 - 11/02/2019 03:59 PM - Sergey Smolov

- Priority changed from Normal to High

#4 - 11/04/2019 12:57 PM - Alexander Kamkin

- Assignee changed from Alexander Kamkin to Alexey Danilov

#5 - 12/03/2019 02:37 PM - Alexey Danilov

- Status changed from New to Resolved

#6 - 04/19/2020 05:55 PM - Sergey Smolov

- Status changed from Resolved to Verified

#7 - 10/02/2020 02:58 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed