Verilog Translator - Bug #9803

ru.ispras.verilog.parser.sample.MulFifoTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator$1.getNode(VerilogElaborator.java:932)

08/29/2019 11:00 PM - Sergey Smolov

Status:	Closed	**Start date:**	08/29/2019
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.2-beta-190909
Platform:			

Description

When running **ru.ispras.verilog.parser.sample.MulFifoTestCase** the following error appears:

```
java.lang.NullPointerException
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator$1.getNode(VerilogElaborator.java:932)
    at ru.ispras.fortress.transformer.Transformer$3.apply(Transformer.java:106)
    at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:169)
    at ru.ispras.fortress.transformer.NodeTransformer.updateNode(NodeTransformer.java:179)
    at ru.ispras.fortress.transformer.NodeTransformer.onVariable(NodeTransformer.java:256)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitVariable(ExprTreeWalker.java:183)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:119)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:160)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
    at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
    at ru.ispras.fortress.transformer.Transformer.transform(Transformer.java:230)
    at ru.ispras.fortress.transformer.Transformer.transform(Transformer.java:213)
    at ru.ispras.fortress.transformer.Transformer.substitute(Transformer.java:111)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.substitute(VerilogElaborator.java:927
)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.generate(VerilogElaborator.java:479)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.start(VerilogElaborator.java:234)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:55)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:187)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.sample.VerilogPrinterTestCase.runTest(VerilogPrinterTestCase.java:
48)
```

History

#1 - 08/30/2019 03:37 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 08/30/2019 03:38 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from Resolved to Verified

#3 - 09/09/2019 06:47 PM - Sergey Smolov

- Published in build set to 0.1.2-beta-190909

- Status changed from Verified to Closed