Verilog Translator - Bug #9775

ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1: Conversion = '''

07/26/2019 11:38 AM - Sergey Smolov

Status:	Closed	**Start date:**	07/26/2019
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

```
java.util.UnknownFormatConversionException: Conversion = '''
    at java.util.Formatter.checkText(Formatter.java:2579)
    at java.util.Formatter.parse(Formatter.java:2565)
    at java.util.Formatter.format(Formatter.java:2501)
    at java.util.Formatter.format(Formatter.java:2455)
    at java.lang.String.format(String.java:2940)
    at ru.ispras.verilog.parser.VerilogLogger.logError(VerilogLogger.java:104)
    at ru.ispras.verilog.parser.VerilogLogger.error(VerilogLogger.java:69)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:199)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:72)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:58)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1(VerilogIeeeTestCase.java:93
3)
```

History

#1 - 09/16/2019 04:18 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from New to Resolved

Missing specifier was added: f5d91cc1

#2 - 09/16/2019 04:18 PM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 10/02/2020 02:58 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed