Verilog Translator - Feature #9774

Case expression/value type casting

07/26/2019 11:37 AM - Mikhail Lebedev

Status:	Closed	**Start date:**	07/26/2019
Priority:	High	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Published in build:	0.1.2-beta-190909		

Description

There can be a situation when an expression in a case and its possible values have different types. For example, vcegar/zaher/zdlx_impl.v_for_pred.v :

```
...
wire [7:0] concat_rep50_3;
...
wire [7:0] concat_rep50_4;
...
case (ID_EX_EXCTRL[4:3])
  concat_rep50_3:
    ALUCtrl =  3'b010;
  concat_rep50_4:
    ALUCtrl =  0;
endcase
```

This situation may lead to an incompatible types error in some tools. Type casting should be performed.

History

#1 - 07/26/2019 11:41 AM - Sergey Smolov

- Target version set to 0.1

#2 - 07/26/2019 06:36 PM - Sergey Smolov

- Status changed from New to Open

#3 - 07/29/2019 07:56 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from Open to Resolved

Fixed in b73ba05f

#4 - 08/30/2019 12:57 PM - Sergey Smolov

- Status changed from Resolved to Verified

#5 - 09/09/2019 06:48 PM - Sergey Smolov

- Published in build set to 0.1.2-beta-190909

- Status changed from Verified to Closed