Verilog Translator - Bug #9594

extra 'BVEXTRACT' operation in right hand side expression in 'assign' block's statement

04/10/2019 04:34 PM - Sergey Smolov

Status:	Closed	**Start date:**	04/10/2019
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.2-beta-190909
Platform:			

Description

In *texas97-tests/ifetch/IFetch.v* module the 'MUX5_30' sub-module is instantiated:

```
MUX5_30    MUX5_30_EarlyPC (
    NewEarlyPC_s1r,
    PCPlus_s1r, {PCChain_s1e[29:26], PCImmedBus_s1e},
    ASBus_s1e[31:2], ExceptionPC_s1[29:0], IStallPC_s1,
    Jump0_s1e, Jump1_s1e, Jump2_s1e, Jump3_s1e, Jump4_s1e);
...
module MUX5_30 (out, in1, in2, in3, in4, in5, sel1, sel2, sel3, sel4, sel5);
    output      [29:0]  out;
    input       [29:0]  in1;
    input       [29:0]  in2;
    input       [29:0]  in3;
    input       [29:0]  in4;
    input       [29:0]  in5;
    input               sel1;
    input               sel2;
    input               sel3;
    input               sel4;
    input               sel5;
    wire        [29:0]  out_b;
    assign
        out_b = (sel5 == 1'b1) ? ~in5 : 30'b0,
        out_b = (sel4 == 1'b1) ? ~in4 : 30'b0,
        out_b = (sel3 == 1'b1) ? ~in3 : 30'b0,
        out_b = (sel2 == 1'b1) ? ~in2 : 30'b0,
        out_b = (sel1 == 1'b1) ? ~in1 : 30'b0;
    assign out = ~out_b;
endmodule
```

The sub-module's instance takes 'ASBus_s1e[31:2]' as 'in3' 30-bit size input. The AST for this assignment looks as follows (run **ru.ispras.verilog.parser.sample.IfetchTestCase** to reproduce)

```
module MUX5_30(out /* DECL: out */, in1 /* DECL: in1 */, in2 /* DECL: in2 */, in3 /* DECL: in3 */,
 in4 /* DECL: in4 */, in5 /* DECL: in5 */, sel1 /* DECL: sel1 */, sel2 /* DECL: sel2 */, sel3 /* D
ECL: sel3 */, sel4 /* DECL: sel4 */, sel5 /* DECL: sel5 */, out /* DECL: out */, in1 /* DECL: in1
 */, in2 /* DECL: in2 */, in3 /* DECL: in3 */, in4 /* DECL: in4 */, in5 /* DECL: in5 */, sel1 /* DE
CL: sel1 */, sel2 /* DECL: sel2 */, sel3 /* DECL: sel3 */, sel4 /* DECL: sel4 */, sel5 /* DECL: se
l5 */);
  output [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:0000000000000000
0000000000000000 /* 00000000000000000000000000000000 */] out;
  input [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:0000000000000000
0000000000000000 /* 00000000000000000000000000000000 */] in1;
  input [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:0000000000000000
0000000000000000 /* 00000000000000000000000000000000 */] in2;
  input [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:0000000000000000
0000000000000000 /* 00000000000000000000000000000000 */] in3;
```

```
  input [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:00000000000000000000000000000000 /* 00000000000000000000000000000000 */] in4;
  input [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:00000000000000000000000000000000 /* 00000000000000000000000000000000 */] in5;
  input sel1;
  input sel2;
  input sel3;
  input sel4;
  input sel5;
  wire [00000000000000000000000000011101 /* 00000000000000000000000000011101 */:00000000000000000000000000000000 /* 00000000000000000000000000000000 */] out_b;
  assign out_b /* DECL: out_b */ = ((sel5 == 1) ?  ~ in5 : 00000000000000000000000000000000) /* (ITE (EQ sel5 1) (BVNOT in5) 00000000000000000000000000000000) */;
  assign out_b /* DECL: out_b */ = ((sel4 == 1) ?  ~ in4 : 00000000000000000000000000000000) /* (ITE (EQ sel4 1) (BVNOT in4) 00000000000000000000000000000000) */;
  assign out_b /* DECL: out_b */ = ((sel3 == 1) ?  ~ in3 : 00000000000000000000000000000000) /* (ITE (EQ sel3 1) (BVNOT in3) 00000000000000000000000000000000) */;
  assign out_b /* DECL: out_b */ = ((sel2 == 1) ?  ~ in2 : 00000000000000000000000000000000) /* (ITE (EQ sel2 1) (BVNOT in2) 00000000000000000000000000000000) */;
  assign out_b /* DECL: out_b */ = ((sel1 == 1) ?  ~ in1 : 00000000000000000000000000000000) /* (ITE (EQ sel1 1) (BVNOT in1) 00000000000000000000000000000000) */;
  assign out /* DECL: out */ =  ~ out_b /* (BVNOT out_b) */;
endmodule

...

assign PCUnitDatapath.MUX5_30_EarlyPC.out_b = ((Jump2_s1e == 1) ?  ~ ASBus_s1e[31:2][31:2] : 00000000000000000000000000000000);
```

When 'getRhsExpression()' method is called for the appropriate VerilogAssignment object, it returns:

```
(ITE (EQ Jump2_s1e 1) (BVNOT (BVEXTRACT 31 2 (BVEXTRACT 31 2 ASBus_s1e))) 00000000000000000000000000000000)
```

An extra "BVEXTRACT" seems to be erroneous here.

History

#1 - 08/16/2019 06:11 PM - Sergey Smolov

- Status changed from New to Open

#2 - 08/19/2019 04:22 PM - Sergey Smolov

Top level module variables does not have hierarchical names, i.e. they don't have *top-module-name* prefix. This comes to the error.

#3 - 08/29/2019 07:51 PM - Alexander Kamkin

- Status changed from Open to Resolved

#4 - 08/29/2019 10:55 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from Resolved to Verified

#5 - 09/09/2019 06:48 PM - Sergey Smolov

- Published in build set to 0.1.2-beta-190909

- Status changed from Verified to Closed