Verilog Translator - Bug #9514

Net declaration assignment is a continuous assignment

03/01/2019 04:44 PM - Mikhail Lebedev

Status:	Closed	**Start date:**	03/01/2019
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.2-beta-190909
Platform:			

Description

According to the Verilog 2005 standard, net declaration assignment is a form of a continuous assignment. Veritrans handles it as an initial value assignment, not as a process.

Chapter 6.1.1 of the standard:

```
... the net declaration assignment, allows a continuous assignment to be placed on a net in the sa
me statement that declares the net.

The following is an example of the net declaration form of a continuous assignment:

wire (strong1, pull0) mynet = enable ;
...
```

See test_06_01_01_1.

History

#1 - 07/26/2019 03:28 PM - Sergey Smolov

- Detected in build changed from svn to master

- % Done changed from 0 to 100

- Assignee changed from Alexander Kamkin to Sergey Smolov

- Status changed from New to Resolved

Done in 7fc1232d

#2 - 07/26/2019 03:30 PM - Mikhail Lebedev

- Status changed from Resolved to Verified

#3 - 09/09/2019 06:49 PM - Sergey Smolov

- Published in build set to 0.1.2-beta-190909

- Target version set to 0.1

- Status changed from Verified to Closed