Retrascope - Feature #9468

HDL parser backend that removes 'initial' processes

01/31/2019 06:13 PM - Sergey Smolov

Status:	Resolved	**Start date:**	01/31/2019
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:	Engine (Parser)	**Estimated time:**	0.00 hour
Target version:	1.0		
Published in build:			

Description

In Verilog, 'initial' blocks are non-synthesizable, as 2005 standard tells.

The backend for HDL parser should be implemented that removes such processes from CFG.

When the 'initial' block contains variables' initialization assignments, these values (if constants!) should be stored at the variables' declarations.

History

#1 - 01/31/2019 06:17 PM - Sergey Smolov

Actually, it is a non 2005 standard issue, but it is supposed to be useful.

#2 - 02/01/2019 06:57 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from New to Resolved

Done in 1c714f47