Verilog Translator - Bug #9282

ru.ispras.verilog.parser.sample.DataMemTestCase: DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr)

09/15/2018 11:58 AM - Sergey Smolov

Status:	Closed	**Start date:**	09/15/2018
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

In the **ru.ispras.verilog.parser.sample.DataMemTestCase** log the following record appears:

```
DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr)
```

It comes from the following fragment of the Verilog '_data_mem.v_' module:

```
wire [`DATA_MEM_ADDR_WIDTH-1 : 0] ram_addr = mem_access_addr[`DATA_MEM_ADDR_WIDTH-1 : 0];
```

The Fortress node that is created from the right hand side expression of this assignment is incorrect, because the first param of BVEXTRACT operation should be greater or equal to the second one.

History

#1 - 09/15/2018 11:58 AM - Sergey Smolov

- Subject changed from Dru.ispras.verilog.parser.sample.DataMemTestCase: DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr) to ru.ispras.verilog.parser.sample.DataMemTestCase: DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr)

#2 - 09/24/2018 05:46 PM - Alexander Kamkin

- Status changed from New to Resolved

#3 - 09/24/2018 06:07 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 09/24/2018 06:07 PM - Sergey Smolov

- Status changed from Verified to Closed