Verilog Translator - Bug #9276

no errors returned for bug-with-macro-containing module

09/12/2018 11:34 AM - Sergey Smolov

Status:	Rejected	**Start date:**	09/12/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The Texas'97 'three_processor.v' module has bugs with macro usages (sometimes "MACRO_NAME" is used, not "`MACRO_NAME"), but the Verilog Translator does not return any error.

Run ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_cache_coherence_three_processor test method.

History

#1 - 09/04/2019 06:17 PM - Sergey Smolov

- Priority changed from High to Normal

#2 - 04/02/2020 04:34 PM - Sergey Smolov

- Status changed from New to Rejected