Verilog Translator - Bug #9255

ru.ispras.verilog.parser.VerilogleeeTestCase.runTest_14_06_04_2_3: no viable alternative

08/31/2018 01:19 PM - Alexander Kamkin

Status:	Closed	**Start date:**	08/31/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

```
module test;
  input a, b;
  output out, out_b;

  specify
    showcancelled out;
    pulsestyle_ondetect out;
    (a => out) = (2,3);
    (b => out) = (4,5);
    showcancelled out_b;
    pulsestyle_ondetect out_b;
    (a => out_b) = (3,4);
    (b => out_b) = (5,6);
  endspecify
  specify
    showcancelled out,out_b;
    pulsestyle_ondetect out,out_b;
    (a => out) = (2,3);
    (b => out) = (4,5);
    (a => out_b) = (3,4);
    (b => out_b) = (5,6);
  endspecify
endmodule
```

History

#1 - 08/31/2018 05:32 PM - Alexander Kamkin

- Status changed from New to Resolved

Typo: KW_PULSESTYPE_ONDETECT -> KW_PULSESTYLE_ONDETECT.

#2 - 08/31/2018 05:49 PM - Alexander Kamkin

- Status changed from Resolved to Closed