Verilog Translator - Bug #9239

ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException

08/20/2018 01:55 PM - Sergey Smolov

Status:	Closed	**Start date:**	08/20/2018
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.1-beta-190722
Platform:			

Description

The tool's error log includes the following:

```
ERROR: ../src/test/verilog/rest-tests/mips16/IF_stage.v line 31:24 extraneous input ''b0' expectin
g SEMI
DEBUG: Expanding macro '8' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '8' ...
DEBUG: End of the token source 'null'
ERROR: ../src/test/verilog/rest-tests/mips16/IF_stage.v line 39:25 extraneous input ''d1' expectin
g SEMI
```

History

#1 - 08/20/2018 02:00 PM - Sergey Smolov

This error appears in **ru.ispras.verilog.parser.sample.IfStageTestCase** test case too.

#2 - 07/26/2019 11:30 AM - Sergey Smolov

- Published in build set to 0.1.1-beta-190722

- % Done changed from 0 to 100

- Status changed from New to Closed