Verilog Translator - Bug #9230

ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PI_BUS_multi_master_bus: java.lang.IllegalArgumentException

08/17/2018 10:42 AM - Sergey Smolov

Status:	Closed	**Start date:**	08/17/2018
Priority:	High	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The test case produces the following exception:

```
java.lang.IllegalArgumentException
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
    at ru.ispras.fortress.util.InvariantChecks.checkFalse(InvariantChecks.java:68)
    at ru.ispras.verilog.parser.VerilogTranslator.exit(VerilogTranslator.java:104)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:193)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:72)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:58)
    at ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PI_BUS_multi_master_bus(VerilogTexa
s97TestCase.java:483)
```

Here is the error log:

```
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 142:22 no viable alternative at input ')'
DEBUG: Expanding macro '3'b001' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 170:27 no viable alternative at input ')'
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b100' ...
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 184:20 no viable alternative at input ')'
DEBUG: Expanding macro '3'b011' ...
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 197:37 no viable alternative at input ')'
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 205:39 no viable alternative at input ')'
DEBUG: Expanding macro '3'b001' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 233:44 no viable alternative at input ')'
DEBUG: Expanding macro '3'b010' ...
DEBUG: End of the token source 'null'
```

```
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 240:40 no viable alternative at input '&&'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 240:51 mismatched input ')' expecting COLON
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 243:20 no viable alternative at input ')'
DEBUG: Expanding macro '3'b001' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b100' ...
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 275:4 mismatched input 'else' expecting KW_END
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 277:28 no viable alternative at input ')'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 277:43 no viable alternative at input ')'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 279:19 mismatched input '=' expecting LPAREN
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 280:19 mismatched input '=' expecting LPAREN
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 281:20 mismatched input '=' expecting LPAREN
DEBUG: Expanding macro '3'b000' ...
ERROR: line 282:15 mismatched input '=' expecting LPAREN
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 286:25 no viable alternative at input ')'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 287:23 mismatched input '=' expecting LPAREN
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 289:23 mismatched input '=' expecting LPAREN
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 290:19 mismatched input '=' expecting LPAREN
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 291:19 mismatched input '=' expecting LPAREN
DEBUG: Expanding macro '3'b011' ...
ERROR: line 292:15 mismatched input '=' expecting LPAREN
DEBUG: End of the token source 'null'
ERROR: /home/ssedai/projects/veritrans/src/test/verilog/texas97-tests/PI_BUS/multi_master/bus.v li
ne 294:7 mismatched input 'end' expecting KW_ENDMODULE
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b001' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b000' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b100' ...
DEBUG: End of the token source 'null'
DEBUG: Expanding macro '3'b100' ...
DEBUG: End of the token source 'null'
ERROR: ru/ispras/verilog/parser/grammar/VerilogTreeBuilder.g: node from line 0:0 mismatched tree n
ode: <mismatched token: [@1039,6991:6993='end',<50>,294:7], resync=modulebus_cont(A,OPC,ACK,LOCK,R
EAD,SEL_0,GNT_0,GNT_1,REQ_0,REQ_1,TOUT,clk);input[0:29]A;input[0:3]OPC;inputACK;inputLOCK;inputREA
D;inputclk;inputREQ_0;inputREQ_1;outputGNT_0;outputGNT_1;outputSEL_0;outputTOUT;wire[2:0]ACK;wireG
NT_0;wireGNT_1;wireSEL_0;wireTOUT;regGNT_reg_0;regGNT_reg_1;reg[0:7]TOUT_cnt;regr_TOUT;regselect_r
eg;regGNT_mux;reg[2:0]state;assignGNT_0=GNT_reg_0;assignGNT_1=GNT_reg_1;assignTOUT=r_TOUT;assignSE
L_0=(A[0]==1)&&(A[1]==1)&&select_reg;initialbeginstate=3'b000;GNT_reg_0=0;GNT_reg_1=0;TOUT_cnt=8'b
00000000;r_TOUT=0;select_reg=0;GNT_mux=0;endalways@(posedgeclk)begincase(state)BUS_IDLE:beginTOUT_
cnt=8'b00000000;if((REQ_0==0)&&(REQ_1==0))state=3'b000;elseif(REQ_0==1&&REQ_1==1)beginGNT_reg_0=~G
NT_mux;GNT_reg_1=GNT_mux;GNT_mux=~GNT_mux;state=3'b001;endelsebeginif(REQ_0==1)GNT_reg_0=1;elseGNT
_reg_1=1;GNT_mux=(REQ_0==1)?1:0;state=3'b001;endendBUS_REQ:beginGNT_reg_0=0;GNT_reg_1=0;if(OPC==0)
select_reg=0;elseselect_reg=1;state=3'b010;endBUS_ADDR:beginif((LOCK==1)&&(OPC==0))beginselect_reg
=0;GNT_reg_0=0;GNT_reg_1=0;state=3'b010;endelseif((LOCK==0)&&(OPC==0))beginif(REQ_0==1||REQ_1==1)b
eginif(REQ_0==1&&REQ_1==1)beginGNT_reg_0=~GNT_mux;GNT_reg_1=GNT_mux;GNT_mux=~GNT_mux;endelsebegini
f(REQ_0==1)GNT_reg_0=1;elseGNT_reg_1=1;GNT_mux=(REQ_0==1)?1:0;endstate=3'b001;endelsebeginGNT_reg_
```

```
0=0;GNT_reg_1=0;TOUT_cnt=8'b00000000;state=3'b000;endendelseif((LOCK==0)&&(!(OPC==0)))beginselect_
reg=0;if(ACK==)beginif(REQ_0==1||REQ_1==1)beginif(REQ_0==1&&REQ_1==1)beginGNT_reg_0=~GNT_mux;GNT_r
eg_1=GNT_mux;GNT_mux=~GNT_mux;endelsebeginif(REQ_0==1)GNT_reg_0=1;elseGNT_reg_1=1;GNT_mux=(REQ_0==
1)?1:0;endstate=3'b001;endelsebeginGNT_reg_0=0;GNT_reg_1=0;TOUT_cnt=8'b00000000;state=3'b000;enden
delseif(ACK==)beginGNT_reg_0=0;GNT_reg_1=0;TOUT_cnt=8'b00000000;state=3'b000;endelsebeginstate=3'b
100;endendelsebeginif(ACK==)select_reg=1;elseselect_reg=0;GNT_reg_0=0;GNT_reg_1=0;state=3'b011;end
endBUS_ADDRDATA:beginTOUT_cnt=TOUT_cnt+1;if(TOUT_cnt==255||ACK==)beginr_TOUT=1;TOUT_cnt=8'b0000000
0;GNT_reg_0=0;GNT_reg_1=0;state=3'b000;endelseif((LOCK==0)&&(ACK==)&&(OPC==0))beginif(REQ_0==1||RE
Q_1==1)beginif(REQ_0==1&&REQ_1==1)beginGNT_reg_0=~GNT_mux;GNT_reg_1=GNT_mux;GNT_mux=~GNT_mux;endel
sebeginif(REQ_0==1)GNT_reg_0=1;elseGNT_reg_1=1;GNT_mux=(REQ_0==1)?1:0;endstate=3'b001;endelsebegin
GNT_reg_0=0;GNT_reg_1=0;TOUT_cnt=8'b00000000;state=3'b000;endendelseif((LOCK==1)&&(ACK==)&&(OPC==0
))beginGNT_reg_0=0;GNT_reg_1=0;select_reg=0;state=3'b010;endelseif(LOCK==0&&ACK==&&OPC!=0)beginsel
ect_reg=0;if(ACK==)beginif(REQ_0==1||REQ_1==1)beginif(REQ_0==1&&REQ_1==1)beginGNT_reg_0=~GNT_mux;G
NT_reg_1=GNT_mux;GNT_mux=~GNT_mux;endelsebeginif(REQ_0==1)GNT_reg_0=1;elseGNT_reg_1=1;GNT_mux=(REQ
_0==1)?1:0;endstate=3'b001;endelsebeginGNT_reg_0=0;GNT_reg_1=0;TOUT_cnt=8'b00000000;state=3'b000;e
ndendelsestate=3'b100;endelsebeginif(!((ACK==)||(ACK==)))beginGNT_reg_0=0;GNT_reg_1=0;select_reg=0
;state=3'b000;endelsebeginif((ACK==)||(OPC==0))select_reg=0;elseselect_reg=1;GNT_reg_0=0;GNT_reg_1
=0;state=3'b011;endendendBUS_DATA:beginTOUT_cnt=TOUT_cnt+1;if> expecting <UP>
```

History

#1 - 08/24/2018 12:30 PM - Sergey Smolov

- % Done changed from 0 to 100

- Assignee changed from Alexander Kamkin to Sergey Smolov

- Status changed from New to Resolved

Fixed in aab96242, but additional error diagnostics is needed.

#2 - 08/24/2018 12:32 PM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 08/24/2018 12:33 PM - Sergey Smolov

- Status changed from Verified to Closed