Verilog Translator - Bug #9226

ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_small_pipeline_pipeline_smv: /src/test/verilog/vcegar-tests/small/pipeline/pipeline_smv.v line 38:10 no viable alternative at input 'property'

08/16/2018 01:34 PM - Sergey Smolov

Status:	Closed	**Start date:**	08/16/2018
Priority:	High	**Due date:**	
Assignee:	Mikhail Lebedev	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The code fragment:

```
always begin
   assert property: ((dataOut == tmp_stageTwo + tmp_stageOne) || (dataOut == 0));
 end
```

produces the following error:

```
ERROR: ../src/test/verilog/vcegar-tests/small/pipeline/pipeline_smv.v line 38:10 no viable alterna
tive at input 'property'
ERROR: ru/ispras/verilog/parser/grammar/VerilogTreeBuilder.g: node from after line 37:8 mismatched
 tree node: <unexpected: [@152,773:780='property',<31>,38:10], resync=assert> expecting <UP>
ERROR: ru/ispras/verilog/parser/grammar/VerilogTreeBuilder.g: node from after line 37:8 mismatched
 tree node: AST_ATTRIBUTES expecting <UP>
ERROR: ru/ispras/verilog/parser/grammar/VerilogTreeBuilder.g: node from after line 37:8 mismatched
 tree node: UP expecting AST_ATTRIBUTES
```

The similar error appears in **ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_sdlx_control1_smv** test case.

History

#1 - 08/16/2018 05:32 PM - Alexander Kamkin

- Assignee changed from Alexander Kamkin to Mikhail Lebedev

Incorrect Verilog code.

#2 - 08/16/2018 06:04 PM - Mikhail Lebedev

- % Done changed from 0 to 100

- Status changed from New to Resolved

Assertions are only available in SystemVerilog. pipeline_smv.v removed.

#3 - 08/16/2018 06:08 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 08/16/2018 06:09 PM - Sergey Smolov

- Status changed from Verified to Closed