Verilog Translator - Bug #9223

ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_pj_icu_icctl1: ERROR: Declaration of 'clk' has not been found

08/15/2018 01:37 PM - Sergey Smolov

Status:	Closed	**Start date:**	08/15/2018
Priority:	High	**Due date:**	
Assignee:	Mikhail Lebedev	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

Run the 'ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_pj_icu_icctl1' test case to reproduce the error.

```
ERROR: Declaration of 'clk' has not been found
1 error(s), 0 warning(s)

java.lang.IllegalArgumentException
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
    at ru.ispras.fortress.util.InvariantChecks.checkFalse(InvariantChecks.java:68)
    at ru.ispras.verilog.parser.VerilogTranslator.exit(VerilogTranslator.java:104)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker
.java:331)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkVariable(VerilogStaticChecker.
java:266)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.access$100(VerilogStaticChecker.jav
a:63)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker$ExprTreeVisitor.onVariable(VerilogS
taticChecker.java:93)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitVariable(ExprTreeWalker.java:183)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:119)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker
.java:390)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker
.java:402)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker
.java:492)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.onDelayedStatementBegin(VerilogStat
icChecker.java:154)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$15.onBegin(VerilogNodeVisitor.java:409)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:700)
    at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:102)
    at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:87)
    at ru.ispras.verilog.parser.VerilogSyntaxBackend.start(VerilogSyntaxBackend.java:80)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:55)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:170)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:72)
    at ru.ispras.verilog.parser.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:58)
    at ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_pj_icu_icctl1(VerilogVcegarTestCase.
java:177)
```

History

#1 - 08/16/2018 12:04 PM - Alexander Kamkin

- Assignee changed from Alexander Kamkin to Mikhail Lebedev

Signal clk is absent.

#2 - 08/16/2018 12:13 PM - Mikhail Lebedev

- % Done changed from 0 to 100

- Status changed from New to Resolved

#3 - 08/16/2018 12:15 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 08/16/2018 12:15 PM - Sergey Smolov

- Status changed from Verified to Closed