Verilog Translator - Bug #9190

ru.ispras.verilog.parser.sample.DescriptorBuffersTestCase: incorrect calculation for string parameter values

08/03/2018 04:08 PM - Sergey Smolov

Status:	Closed	**Start date:**	08/03/2018
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The testcase output contains the following description for 'OUTDATA_REG' parameter:

```
Override parameter: the_write_command_FIFO.the_dp_ram.ram_model.OUTDATA_REG = the_write_command_FI
FO.the_dp_ram.outdata_reg_b = Data[type=(BIT_VECTOR 64), value=0010001000110000010010110100001101
0111101001100010000110010010]
```

This parameter is of string type, as it is written in altera_msgdma_mod/dispatcher/altsyncram_model.v:

```
parameter OUTDATA_REG = "UNREGISTERED"
```

History

#1 - 08/06/2018 02:52 PM - Alexander Kamkin

The value is correct (not taking the quotes into account):

```
7: 00100010 22 "
6: 00110000 30 0
5: 01001011 4B K
4: 01000011 43 C
3: 01001111 4F 0
2: 01001100 4C L
1: 01000011 43 C
0: 00100010 22 "
```

#2 - 08/06/2018 03:03 PM - Alexander Kamkin

- Status changed from New to Open

String literal encoding has been fixed:

```
5: 00110000 30 0
4: 01001011 4B K
3: 01000011 43 C
2: 01001111 4F O
1: 01001100 4C L
0: 01000011 43 C
```

#3 - 08/06/2018 05:03 PM - Alexander Kamkin

A new test case GenerateTestCase has been added. It seems that the problem is in handing generate constructs of nested blocks. The constructs are ignored.

#4 - 08/06/2018 07:25 PM - Alexander Kamkin

- Status changed from Open to Resolved

Elaboration logic has been fixed.

#5 - 08/07/2018 06:00 PM - Sergey Smolov

- Status changed from Resolved to Verified

#6 - 08/07/2018 06:00 PM - Sergey Smolov

- Status changed from Verified to Closed