Verilog Translator - Bug #9182

ru.ispras.verilog.parser.sample.MulFifoTestCase: java.lang.IllegalStateException: Parameter is not a value: i

08/01/2018 02:41 PM - Sergey Smolov

Status:	Closed	**Start date:**	08/01/2018
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

Running the described testcase causes an exception with the following stack trace:

```
java.lang.IllegalStateException: Parameter is not a value: i
    at ru.ispras.fortress.expression.NodeOperation.getParams(NodeOperation.java:260)
    at ru.ispras.fortress.expression.NodeOperation.getDataType(NodeOperation.java:196)
    at ru.ispras.fortress.expression.Node.isType(Node.java:177)
    at ru.ispras.fortress.expression.ExprUtils.isType(ExprUtils.java:84)
    at ru.ispras.verilog.parser.processor.VerilogExprTransformer$2.apply(VerilogExprTransformer.ja
va:166)
    at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:169)
    at ru.ispras.fortress.transformer.NodeTransformer.onOperationEnd(NodeTransformer.java:229)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:173)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:160)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
    at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
    at ru.ispras.fortress.transformer.Transformer.transform(Transformer.java:230)
    at ru.ispras.verilog.parser.processor.VerilogExprTransformer.transform(VerilogExprTransformer.
java:62)
    at ru.ispras.verilog.parser.elaborator.VerilogTransformer.transform(VerilogTransformer.java:18
0)
    at ru.ispras.verilog.parser.elaborator.VerilogTransformer.onIfStatementBegin(VerilogTransforme
r.java:109)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$20.onBegin(VerilogNodeVisitor.java:469)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:700)
    at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:100)
    at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:85)
    at ru.ispras.verilog.parser.elaborator.VerilogTransformer.run(VerilogTransformer.java:54)
    at ru.ispras.verilog.parser.elaborator.VerilogVariableSubstitutor.transform(VerilogVariableSub
stitutor.java:44)
    at ru.ispras.verilog.parser.elaborator.VerilogInstantiator.instantiate(VerilogInstantiator.jav
a:106)
    at ru.ispras.verilog.parser.elaborator.VerilogInstantiator.instantiateProcess(VerilogInstantia
tor.java:84)
    at ru.ispras.verilog.parser.elaborator.VerilogDesign$1$1.next(VerilogDesign.java:181)
    at ru.ispras.verilog.parser.elaborator.VerilogDesign$1$1.next(VerilogDesign.java:169)
    at ru.ispras.verilog.parser.sample.VerilogDesignPrinter.start(VerilogDesignPrinter.java:36)
    at ru.ispras.verilog.parser.VerilogDesignBackends.start(VerilogDesignBackends.java:56)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:169)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.sample.VerilogPrinterTestCase.runTest(VerilogPrinterTestCase.java:
48)
```

The problem seems to be connected with the following Verilog code:

```
generate
    genvar i;
    for (i=0; i!=(1 << FCOUNT_SIZE); i=i+1) begin
        myfifo #(ADDR_SIZE,DATA_SIZE) one_fifo(
        .DO(DO_tmp[i]),
        .DO_VAL(DO_VAL_tmp[i]),
        .IS_EMPTY(IS_EMPTY[i]),
        .IS_FULL(IS_FULL[i]),
        .CLK(CLK),
        .RST(RST),
        .DI(DI),
        .CE_RD(CE_RD_tmp[i]),
        .CE_WR(CE_WR_tmp[i])
        );

        assign CE_WR_tmp[i] = (WR_A == i) ? CE_WR : 1'b0;
        assign CE_RD_tmp[i] = (RD_A == i) ? CE_RD : 1'b0;

        always @(posedge CLK) begin
            if(DO_VAL_tmp[i]) begin
                DO <= DO_tmp[i];
            end
        end

    end
endgenerate
```

History

#1 - 08/01/2018 02:42 PM - Sergey Smolov

- Priority changed from Normal to High

#2 - 08/06/2018 07:28 PM - Alexander Kamkin

The DescriptorBuffersTestCase causes the same problem:

```
java.lang.IllegalStateException: Parameter is not a value: the_read_command_FIFO.the_dp_ram.width_byteena_a
```

#3 - 08/07/2018 03:14 PM - Alexander Kamkin

The problem is as follows: if there is a binding var -> expr(param), then VerilogVariableSubstitutor replaces var with expr(param) and does not replace param to the corresponding value. It seems that two-level replacement is required.

#4 - 08/07/2018 04:56 PM - Alexander Kamkin

- Status changed from New to Resolved

#5 - 08/08/2018 12:54 PM - Sergey Smolov

- Status changed from Resolved to Verified

#6 - 08/08/2018 12:54 PM - Sergey Smolov

- Status changed from Verified to Closed