Verilog Translator - Feature #8874

mapping from instance variables to their code entries

05/15/2018 03:19 PM - Sergey Smolov

Status:	Closed	**Start date:**	05/15/2018
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Published in build:			

Description

Those variables that have "flattened" hierarchical names (that are built on the base of instance name) should be somehow linked with their code entries.
A design-level map would be very helpful.

History

#1 - 05/28/2018 04:23 PM - Sergey Smolov

- Status changed from New to Closed