Verilog Translator - Bug #8864

VerilogIeeeTestCase.runTest_17_10_02_1_i: java.lang.IllegalArgumentException

05/07/2018 12:40 PM - Sergey Smolov

Status:	Closed	**Start date:**	05/07/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The stack trace:

```
java.lang.IllegalArgumentException
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
    at ru.ispras.fortress.util.InvariantChecks.checkNotNull(InvariantChecks.java:95)
    at ru.ispras.verilog.parser.processor.VerilogExprTransformer$2.apply(VerilogExprTransformer.ja
va:169)
    at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:166)
    at ru.ispras.fortress.transformer.NodeTransformer.onOperationEnd(NodeTransformer.java:226)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:173)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
    at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
    at ru.ispras.fortress.transformer.Transformer.transform(Transformer.java:230)
    at ru.ispras.verilog.parser.processor.VerilogExprTransformer.transform(VerilogExprTransformer.
java:62)
    at ru.ispras.verilog.parser.elaborator.VerilogTransformer.transform(VerilogTransformer.java:15
9)
    at ru.ispras.verilog.parser.elaborator.VerilogTransformer.onIfStatementBegin(VerilogTransforme
r.java:96)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$20.onBegin(VerilogNodeVisitor.java:469)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:700)
    at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:100)
    at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:85)
    at ru.ispras.verilog.parser.elaborator.VerilogTransformer.run(VerilogTransformer.java:53)
    at ru.ispras.verilog.parser.elaborator.VerilogVariableSubstitutor.transform(VerilogVariableSub
stitutor.java:44)
    at ru.ispras.verilog.parser.elaborator.VerilogInstantiator.instantiateProcess(VerilogInstantia
tor.java:88)
    at ru.ispras.verilog.parser.elaborator.VerilogDesign$1$1.next(VerilogDesign.java:185)
    at ru.ispras.verilog.parser.elaborator.VerilogDesign$1$1.next(VerilogDesign.java:173)
    at ru.ispras.verilog.parser.sample.VerilogDesignPrinter.start(VerilogDesignPrinter.java:36)
    at ru.ispras.verilog.parser.VerilogDesignBackends.start(VerilogDesignBackends.java:56)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:169)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1813)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1799)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_17_10_02_1_i(VerilogIeeeTestCase.java:
1580)
```

The target Verilog module:

```
// IEEE Std 1364-2005
//   17. System tasks and functions
//     17.10 Command line input
//       17.10.2 $value$plusargs (user_string, variable)
```

```
`define STRING reg [1024 * 8:1]

module goodtasks;
  `STRING str;
  integer int;
  reg [31:0] vect;
  real realvar;

  initial begin
    if ($value$plusargs ("TEST=%d",int))
      $display ("value was %d",int);
    else
      $display ("+TEST= not found");
      #100 $finish ;
    end
endmodule

module ieee1364_example;
  real frequency;
  reg [8*32:1] testname;
  reg [64*8:1] pstring;
  reg clk;

  initial begin
  if  ( $value$plusargs ("TESTNAME=%s",testname))
  begin
    $display (" TESTNAME= %s.",testname);
    $finish;
    end
  if (!( $value$plusargs ("FREQ+%0F",frequency)))
    frequency = 8.33333; // 166 MHz
  $display ("frequency = %f",frequency);
  pstring = "TEST%d";
  if ( $value$plusargs (pstring, testname))
    $display ("Running test number %0d.", testname);
end
endmodule
```

History

#1 - 09/06/2018 01:25 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 09/06/2018 01:47 PM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 09/06/2018 01:48 PM - Sergey Smolov

- Status changed from Verified to Closed