Verilog Translator - Bug #8859

VerilogleeeTestCase.runTest_12_04_02_3: java.lang.NullPointerException

05/07/2018 12:15 PM - Sergey Smolov

Status:	Closed	**Start date:**	05/07/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The stack trace:

```
java.lang.NullPointerException
    at ru.ispras.verilog.parser.model.basis.VerilogLiteral.getBoolean(VerilogLiteral.java:295)
    at ru.ispras.verilog.parser.model.util.ModelUtils.newBoolean(ModelUtils.java:89)
    at ru.ispras.verilog.parser.calculator.VerilogOperations$3.calculate(VerilogOperations.java:86
)
    at ru.ispras.fortress.calculator.OperationGroup.calculate(OperationGroup.java:145)
    at ru.ispras.fortress.transformer.Reducer$OperationRule.apply(Reducer.java:148)
    at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:166)
    at ru.ispras.fortress.transformer.NodeTransformer.updateNode(NodeTransformer.java:176)
    at ru.ispras.fortress.transformer.NodeTransformer.onOperationEnd(NodeTransformer.java:224)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:173)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
    at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
    at ru.ispras.fortress.transformer.Reducer.reduce(Reducer.java:184)
    at ru.ispras.verilog.parser.processor.VerilogExprTransformer.evaluate(VerilogExprTransformer.j
ava:93)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.evaluate(VerilogElaborator.java:698)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.generate(VerilogElaborator.java:413)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.start(VerilogElaborator.java:192)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:56)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:163)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1813)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1799)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_12_04_02_3(VerilogIeeeTestCase.java:10
84)
```

The target Verilog module:

```
// IEEE Std 1364-2005
//   12. Hierarchical structures
//     12.4 Generate constructs
//       12.4.2 Conditional generate constructs
//         Generate with a case to handle widths less than 3.

module adder_1bit(co, sum, a, b, ci);
  input co, sum, a, b, ci;
endmodule

module adder_2bit(co, sum, a, b, ci);
  input co, sum, a, b, ci;
endmodule

module adder_cla(co, sum, a, b, ci);
```

```
  input co, sum, a, b, ci;
endmodule

module test;
  parameter WIDTH = 0;
  reg co, sum, a, b, ci;
  generate
    case (WIDTH)
      1: begin : adder        // 1-bit adder implementation
        adder_1bit x1(co, sum, a, b, ci);
      end
      2: begin : adder        // 2-bit adder implementation
        adder_2bit x1(co, sum, a, b, ci);
      end
      default : begin : adder // others - carry look-ahead adder
        adder_cla #(WIDTH) x1(co, sum, a, b, ci);
      end
    endcase
    // The hierarchical instance name is adder.x1
  endgenerate

endmodule
```

History

#1 - 08/09/2018 06:59 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 08/10/2018 10:32 AM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 08/10/2018 10:32 AM - Sergey Smolov

- Status changed from Verified to Closed