

Verilog Translator - Bug #8856

VerilogIeeeTestCase.runTest_10_04_05_1: java.lang.IllegalArgumentException

05/07/2018 12:03 PM - Sergey Smolov

Status:	Closed	Start date:	05/07/2018
Priority:	Normal	Due date:	
Assignee:	Alexander Kamkin	% Done:	0%
Category:		Estimated time:	0.00 hour
Target version:	0.1	Published in build:	
Detected in build:	master		
Platform:			

Description

The stack trace:

```
java.lang.IllegalArgumentException
  at ru.ispras.fortress.util.InvariantChecks.checkTrue (InvariantChecks.java:53)
  at ru.ispras.fortress.util.InvariantChecks.checkTrue (InvariantChecks.java:38)
  at ru.ispras.fortress.util.InvariantChecks.checkNotNull (InvariantChecks.java:95)
  at ru.ispras.verilog.parser.elaborator.VerilogDesign$Builder.addParameter (VerilogDesign.java:64)
  at ru.ispras.verilog.parser.elaborator.VerilogElaborator.defineParameter (VerilogElaborator.java:636)
  at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createBindings (VerilogElaborator.java:515)
  at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createBindings (VerilogElaborator.java:481)
  at ru.ispras.verilog.parser.elaborator.VerilogElaborator.expand (VerilogElaborator.java:275)
  at ru.ispras.verilog.parser.elaborator.VerilogElaborator.start (VerilogElaborator.java:181)
  at ru.ispras.verilog.parser.VerilogSyntaxBackends.start (VerilogSyntaxBackends.java:56)
  at ru.ispras.verilog.parser.VerilogTranslator.start (VerilogTranslator.java:163)
  at ru.ispras.verilog.parser.sample.VerilogPrinter.main (VerilogPrinter.java:45)
  at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest (VerilogIeeeTestCase.java:1813)
  at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest (VerilogIeeeTestCase.java:1799)
  at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_05_1 (VerilogIeeeTestCase.java:929)
```

The target Verilog module:

```
// IEEE Std 1364-2005
// 10. Tasks and functions
// 10.4 Functions and function calling
// 10.4.5 Use of constant functions
// This example defines a function called clogb2 that returns an integer with the value of
// the ceiling of the log base 2.

module ram_model (address, write, chip_select, data);
  parameter data_width = 8;
  parameter ram_depth = 256;
  localparam addr_width = clogb2(ram_depth);
  input [addr_width - 1:0] address;
  input write, chip_select;
  inout [data_width - 1:0] data;

  //define the clogb2 function
  function integer clogb2;
    input [31:0] value;
    begin
      value = value - 1;
      for (clogb2 = 0; value > 0; clogb2 = clogb2 + 1)
```

```
        value = value >> 1;
    end
endfunction

reg [data_width - 1:0] data_store[0:ram_depth - 1];

//the rest of the ram model
endmodule
```

History

#1 - 09/04/2018 04:35 PM - Alexander Kamkin

- Status changed from *New* to *Resolved*

#2 - 09/04/2018 06:04 PM - Sergey Smolov

- Status changed from *Resolved* to *Verified*

#3 - 09/04/2018 06:04 PM - Sergey Smolov

- Status changed from *Verified* to *Closed*