Verilog Translator - Bug #8852

VerilogIeeeTestCase.runTest_05_01_14_4: java.lang.NullPointerException

05/07/2018 11:17 AM - Sergey Smolov

Status:	Closed	**Start date:**	05/07/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The stack trace:

```
java.lang.NullPointerException
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker
.java:326)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker
.java:353)
    at ru.ispras.verilog.parser.processor.VerilogStaticChecker.onAssignStatementBegin(VerilogStati
cChecker.java:106)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$3.onBegin(VerilogNodeVisitor.java:265)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:700)
    at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:100)
    at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:85)
    at ru.ispras.verilog.parser.VerilogSyntaxBackend.start(VerilogSyntaxBackend.java:80)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:56)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:163)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1813)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1799)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_05_01_14_4(VerilogIeeeTestCase.java:28
3)
```

The target Verilog module:

```
// IEEE Std 1364-2005
//   5. Expressions
//    5.1 Operators
//      5.1.14 Concatenations
//        Example 4

module test;
  reg [7:0] result;
  reg [1:0] y, w;

  function [1:0] func;
    input [1:0] x;
    begin
      func = x;
    end
  endfunction

  initial begin
    // When a replication expression is evaluated, the operands shall be evaluated exactly once,
    // even if the replication constant is zero. For example:
    result = {4{func(w)}};

    // would be computed as
```

```
    y = func(w) ;
    result = {y, y, y, y};
  end
endmodule
```

History

#1 - 05/07/2018 11:36 AM - Sergey Smolov

Same error comes for:

1. VerilogIeeeTestCase.runTest_06_01_02_1 testcase
   The target Verilog module:

```
// IEEE Std 1364-2005
//   6. Expressions
//     6.1 Continuous assignments
//       6.1.2 The continuous assignment statement
//         The following is an example of a continuous assignment to a net that
//         has been previously declared

module test;
  reg enable;
  wire  mynet;
  assign (strong1, pull0) mynet = enable;
endmodule
```

2. VerilogIeeeTestCase.runTest_09_03_01_1 testcase
   The target Verilog module:

```
// IEEE Std 1364-2005
//   9. Behavioral modeling
//     9.3 Procedural continuous assignments
//       9.3.1 The assign and deassign procedural statements
//         The following example shows a use of the assign and deassign procedural statements in a
//         behavioral description of a D-type flip-flop with preset and clear inputs.

module dff (q, d, clear, preset, clock);
  output q;
  input d, clear, preset, clock;
  reg q;
  always @(clear or preset)
    if (!clear)
      assign q = 0;
    else if (!preset)
      assign q = 1;
    else
      deassign q;
  always @( posedge clock)
    q = d;
endmodule
```

#2 - 08/16/2018 05:34 PM - Alexander Kamkin

- Status changed from New to Resolved

#3 - 08/16/2018 05:45 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 08/16/2018 05:45 PM - Sergey Smolov

- Status changed from Verified to Closed