Verilog Translator - Bug #8849

VerilogIeeeTestCase.runTest_04_10_01_1 [floating point parameters]: java.lang.IllegalArgumentException

05/07/2018 10:39 AM - Sergey Smolov

Status:	Closed	**Start date:**	05/07/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

The tool stack trace:

```
java.lang.IllegalArgumentException
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
    at ru.ispras.verilog.parser.model.basis.VerilogLiteral.getBitVector(VerilogLiteral.java:274)
    at ru.ispras.verilog.parser.calculator.VerilogOperations$9.calculate(VerilogOperations.java:20
2)
    at ru.ispras.fortress.calculator.OperationGroup.calculate(OperationGroup.java:145)
    at ru.ispras.fortress.transformer.Reducer$OperationRule.apply(Reducer.java:148)
    at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:166)
    at ru.ispras.fortress.transformer.NodeTransformer.updateNode(NodeTransformer.java:176)
    at ru.ispras.fortress.transformer.NodeTransformer.onOperationEnd(NodeTransformer.java:224)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:173)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:160)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
    at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
    at ru.ispras.fortress.transformer.Reducer.reduce(Reducer.java:184)
    at ru.ispras.verilog.parser.processor.VerilogExprTransformer.evaluate(VerilogExprTransformer.j
ava:93)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.evaluate(VerilogElaborator.java:698)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.defineParameter(VerilogElaborator.jav
a:626)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createBindings(VerilogElaborator.java
:515)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createBindings(VerilogElaborator.java
:481)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.expand(VerilogElaborator.java:275)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.start(VerilogElaborator.java:181)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:56)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:163)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1813)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest(VerilogIeeeTestCase.java:1799)
    at ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_04_10_01_1(VerilogIeeeTestCase.java:18
3)
```

The target Verilog module:

```
// IEEE Std 1364-2005
//   4. Data types
//    4.10 Parameters
//      4.10.1 Module parameters
module test;
```

```
  parameter msb = 7;                  // defines msb as a constant value 7
  parameter e = 25, f = 9;            // defines two constant numbers
  parameter r = 5.7;                  // declares r as a real parameter
  parameter byte_size = 8,
            byte_mask = byte_size - 1;
  parameter average_delay = (r + f) / 2;
  parameter signed [3:0] mux_selector = 0;
  parameter real r1 = 3.5e17;
  parameter p1 = 13'h7e;
  parameter [31:0] dec_const = 1'b1; // value converted to 32 bits
  parameter newconst = 3'h4;          // implied range of [2:0]
  parameter newconst2 = 4;             // implied range of at least [31:0]
endmodule
```

History

#1 - 05/07/2018 10:56 AM - Sergey Smolov

Same error comes for *VerilogIeeeTestCase.runTest_05_01_05_2* test case.
The target Verilog module:

```
// IEEE Std 1364-2005
//   5. Expressions
//    5.1 Operators
//      5.1.5 Arithmetic operators
//        Table 5-8 - Examples of modulus and power operators
module test;
  reg result;

  initial begin
    result = 10 % 3;        // Result:   1; Comments: 10/3 yields a remainder of 1.
    result = 11 % 3;        // Result:   2; Comments: 11/3 yields a remainder of 2.
    result = 12 % 3;        // Result:   0; Comments: 12/3 yields no remainder.
    result = -10 % 3;       // Result:  -1; Comments: The result takes the sign of the first operand.
    result = 11 % -3;       // Result:   2; Comments: The result takes the sign of the first operand
    result = -4'd12 % 3;    // Result:   1; Comments: -4'd12 is seen as a large positive number that leaves a
remainder of 1 when divided by 3.
    result = 3 ** 2;        // Result:   9; Comments: 3 * 3
    result = 2 ** 3;        // Result:   8; Comments: 2 * 2 * 2
    result = 2 ** 0;        // Result:   1; Comments: Anything to the zero exponent is 1.
    result = 0 ** 0;        // Result:   1; Comments: Zero to the zero exponent is also 1.
    result = 2.0 ** -3'sb1; // Result: 0.5; Comments: 2.0 is real, giving real reciprocal.
    result = 2 ** -3 'sb1;  // Result:   0; Comments: 2 ** -1 = 1/2. Integer division truncates to zero.
    result = 0 ** -1 'bx;   // Result:   0; Comments: 0 ** -1 = 1/0. Integer division by zero is 'bx.
    result = 9 ** 0.5;      // Result: 3.0; Comments: Real square root.
    result = 9.0 ** (1/2);  // Result: 1.0; Comments: Integer division truncates exponent to zero.
    result = -3.0 ** 2.0;   // Result: 9.0; Comments: Defined because real 2.0 is still integral value.
  end
endmodule
```

#2 - 08/09/2018 07:38 PM - Alexander Kamkin

- Subject changed from VerilogIeeeTestCase.runTest_04_10_01_1: java.lang.IllegalArgumentException to VerilogIeeeTestCase.runTest_04_10_01_1 [floating point parameters]: java.lang.IllegalArgumentException

#3 - 09/16/2019 05:46 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from New to Resolved

Fixed in d632d962

#4 - 09/16/2019 05:52 PM - Sergey Smolov

- Status changed from Resolved to Verified

#5 - 10/02/2020 02:55 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed