Verilog Translator - Bug #8830

verilog2smv-vis-benchmarks/Silver-bcu fails with IllegalArgumentException

04/13/2018 03:24 PM - Mikhail Lebedev

Status:	Closed	**Start date:**	04/13/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

This error appears when running ru.ispras.verilog.parser.sample.vis.VisBcuVerilogPrinterTestCase in the Retrascope MC Benchmark project.
The corresponding Verilog file:

retrascope-mc-benchmark/src/main/verilog/verilog2smv-vis-benchmarks/Silver-bcu/bcuvis32.v

The error:

```
java.lang.IllegalArgumentException
at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
at ru.ispras.fortress.util.InvariantChecks.checkNotNull(InvariantChecks.java:95)
at ru.ispras.verilog.parser.model.util.ModelUtils.getNode(ModelUtils.java:147)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_primary(VerilogTreeBuilder.java:6345)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_operation(VerilogTreeBuilder.java:6178)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_expression(VerilogTreeBuilder.java:6033)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_binary_operation(VerilogTreeBuilder.java:6893)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_operation(VerilogTreeBuilder.java:6198)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_expression(VerilogTreeBuilder.java:6033)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_if_statement(VerilogTreeBuilder.java:4646)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_statement(VerilogTreeBuilder.java:4062)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_block_statement(VerilogTreeBuilder.java:5144)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_statement(VerilogTreeBuilder.java:4092)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_procedure(VerilogTreeBuilder.java:3561)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_item(VerilogTreeBuilder.java:958)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_module(VerilogTreeBuilder.java:666)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_root(VerilogTreeBuilder.java:508)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.startRule(VerilogTreeBuilder.java:458)
at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:240)
at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:245)
at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:256)
at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:260)
at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:162)
```

Module name: bcu

History

#1 - 06/27/2018 07:13 PM - Mikhail Lebedev

- Status changed from New to Resolved

#2 - 06/27/2018 07:13 PM - Mikhail Lebedev

- Status changed from Resolved to Verified

#3 - 07/27/2018 05:32 PM - Sergey Smolov

- Status changed from Verified to Closed