Verilog Translator - Bug #8829

vcegar-benchmarks/usb_phy fails with IllegalArgumentException

04/13/2018 03:16 PM - Mikhail Lebedev

Status:	Closed	**Start date:**	04/13/2018
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

This error appears when running ru.ispras.verilog.parser.sample.vcegar.VcegarUsbPhyVerilogPrinterTestCase in the Retrascope MC Benchmark project.
The corresponding Verilog file:

retrascope-mc-benchmark/src/main/verilog/vcegar-benchmarks/usb_phy/usb_phy_1.v

The error:

```
java.lang.IllegalArgumentException
at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:38)
at ru.ispras.fortress.util.InvariantChecks.checkNotNull(InvariantChecks.java:95)
at ru.ispras.verilog.parser.model.util.ModelUtils.getNode(ModelUtils.java:147)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_primary(VerilogTreeBuilder.java:6345)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_operation(VerilogTreeBuilder.java:6178)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_expression(VerilogTreeBuilder.java:6033)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_port_connection(VerilogTreeBuilder.java:3395)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_instantiation(VerilogTreeBuilder.java:3320)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_item(VerilogTreeBuilder.java:948)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_module(VerilogTreeBuilder.java:666)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_root(VerilogTreeBuilder.java:508)
at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.startRule(VerilogTreeBuilder.java:458)
at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:240)
at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:245)
at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:256)
at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:260)
at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:162)
```

Module name: main

History

#1 - 04/17/2018 06:29 PM - Alexander Kamkin

Implicit declaration in instantiation.

#2 - 06/19/2018 01:04 PM - Sergey Smolov

- Detected in build changed from svn to master

- Priority changed from Normal to High

This error appears in other designs, like src/main/verilog/vcegar-benchmarks/cache_coherence/three_processor_bin_2.v

#3 - 08/08/2018 07:29 PM - Sergey Smolov

- Status changed from New to Resolved

The ru.ispras.verilog.parser.sample.vcegar.VcegarUsbPhyVerilogPrinterTestCase passes now.

#4 - 08/24/2018 12:56 PM - Alexander Kamkin

- Status changed from Resolved to Closed