Verilog Translator - Bug #8828

vcegar-benchmarks/pi_bus fails with IndexOutOfBoundsException

04/13/2018 03:11 PM - Mikhail Lebedev

Status:	Closed	**Start date:**	04/13/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

This error appears when running ru.ispras.verilog.parser.sample.vcegar.VcegarPiBusVerilogPrinterTestCase in the Retrascope MC Benchmark project.
The corresponding Verilog file:

retrascope-mc-benchmark/src/main/verilog/vcegar-benchmarks/pi_bus/main_1.v

The error:

```
java.lang.IndexOutOfBoundsException: 4294967267 is out of bounds.
at ru.ispras.fortress.expression.NodeOperation.getParams(NodeOperation.java:273)
at ru.ispras.fortress.expression.NodeOperation.getDataType(NodeOperation.java:196)
at ru.ispras.verilog.parser.processor.VerilogExprTransformer$4.apply(VerilogExprTransformer.java:241)
at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:166)
at ru.ispras.fortress.transformer.NodeTransformer.onOperationEnd(NodeTransformer.java:226)
at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:173)
at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:160)
at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:160)
at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
at ru.ispras.fortress.transformer.Transformer.transform(Transformer.java:230)
at ru.ispras.verilog.parser.processor.VerilogExprTransformer.transform(VerilogExprTransformer.java:61)
at ru.ispras.verilog.parser.processor.VerilogProcessorContextUtils.reduceExpression(VerilogProcessorContextUtils.java:69)
at ru.ispras.verilog.parser.processor.VerilogStaticChecker.reduce(VerilogStaticChecker.java:579)
at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker.java:349)
at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker.java:366)
at ru.ispras.verilog.parser.processor.VerilogStaticChecker.checkReference(VerilogStaticChecker.java:388)
at ru.ispras.verilog.parser.processor.VerilogStaticChecker.onAssignBegin(VerilogStaticChecker.java:106)
at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$2.onBegin(VerilogNodeVisitor.java:253)
at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:700)
at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:100)
at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:85)
at ru.ispras.verilog.parser.VerilogSyntaxBackend.start(VerilogSyntaxBackend.java:80)
at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:56)
at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:163)
```

History

#1 - 04/13/2018 03:17 PM - Mikhail Lebedev

Module name: main

#2 - 04/17/2018 05:24 PM - Alexander Kamkin

- Status changed from New to Resolved

#3 - 05/11/2018 03:59 PM - Mikhail Lebedev

- % Done changed from 0 to 100

- Status changed from Resolved to Verified

#4 - 05/28/2018 04:10 PM - Alexander Kamkin

- Status changed from Verified to Closed