Verilog Translator - Bug #8797

Error when using multiple includes

04/03/2018 03:17 PM - Alexander Kamkin

Status:	New	**Start date:**	04/03/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

Something strange happens when including several files in a raw.

History

#1 - 04/03/2018 05:55 PM - Alexander Kamkin

Crash has been fixed. However, the order of inclusion is incorrect (should be reversed).