Verilog Translator - Bug #8796

Error when handling incorrect tokens under ifdef

04/03/2018 12:33 PM - Alexander Kamkin

Status:	Closed	**Start date:**	04/03/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

```
Including file 'C:\SVN\veritrans\src\test\verilog\ieee-tests\test_3_5_1_3.v' ...
veritrans\src\test\verilog\ieee-tests\test_3_5_1_3.v line 24:23 mismatched character '-' expecting
 set null
```

History

#1 - 09/07/2018 05:08 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 09/07/2018 05:09 PM - Alexander Kamkin

- Status changed from Resolved to Closed