Verilog Translator - Bug #8791

Error when using escaped identifiers

03/29/2018 01:33 PM - Alexander Kamkin

Status:	Closed	**Start date:**	03/29/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

```
veritrans\src\test\verilog\ieee-tests\test_3_7_1_1.v line 23:2 no viable alternative at input 'reg
'
veritrans\src\test\verilog\ieee-tests\test_3_7_1_1.v line 23:2 mismatched input 'reg' expecting LP
AREN
...
```

History

#1 - 04/03/2018 02:25 PM - Alexander Kamkin

- Status changed from New to Resolved

Each escaped identifiers should end with a whitespace. The grammar has been updated.

#2 - 04/09/2018 02:14 PM - Alexander Kamkin

- Status changed from Resolved to Closed