Verilog Translator - Bug #8789

Error when using special symbols in strings

03/29/2018 01:22 PM - Alexander Kamkin

Status:	Closed	**Start date:**	03/29/2018
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

Unsupported "\""

```
veritrans\src\test\verilog\ieee-tests\test_3_6_3_1.v line 25:27 mismatched character '\n' expectin
g '"'
veritrans\src\test\verilog\ieee-tests\test_3_6_3_1.v line 26:2 missing SEMI at 'reg'
```

History

#1 - 08/24/2018 12:42 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 08/24/2018 12:56 PM - Alexander Kamkin

- Status changed from Resolved to Closed