Verilog Translator - Bug #8786

ru.ispras.verilog.parser.sample.FifoTestbenchTestCase fails

03/27/2018 05:38 PM - Sergey Smolov

Status:	Closed	**Start date:**	03/27/2018
Priority:	High	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	
Platform:			

Description

The same problem, that makes this test to be failed, appears while running Retrascope at Jenkins server with the following parameters:

```
/srv/jenkins/workspace/Retrascope/build/resources/test/fifo/fifo_testbench.v
 --target cfg-iface
 --include-path /srv/jenkins/workspace/Retrascope/build/resources/test/fifo
 --module-name fifo_testbench
 --engine cfg-cfginterface-extractor
```

Here comes an error like:

```
java.lang.IllegalArgumentException: Module 'fifo' cannot be found
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkNotNull(InvariantChecks.java:109)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.expand(VerilogElaborator.java:334)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.start(VerilogElaborator.java:176)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:56)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:163)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:51)
    at ru.ispras.verilog.parser.sample.VerilogPrinterTestCase.runTest(VerilogPrinterTestCase.java:
48)
```

History

#1 - 03/28/2018 11:51 AM - Sergey Smolov

- % Done changed from 0 to 100

- Assignee changed from Alexander Kamkin to Sergey Smolov

- Status changed from New to Resolved

"`include" directives were added to top Verilog module for correct processing.

#2 - 03/28/2018 11:53 AM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 04/09/2018 02:14 PM - Alexander Kamkin

- Status changed from Verified to Closed