Verilog Translator - Bug #6355

src/test/verilog/fifo/fifo_testbench.v: NullPointerException

10/16/2015 02:24 PM - Sergey Smolov

Status:	Closed	**Start date:**	10/16/2015
Priority:	High	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

While running VerilogPrinter on src/test/verilog/fifo/fifo_testbench.v the following error appears:

```
Including file 'src/test/verilog/fifo/fifo_testbench.v'
java.lang.NullPointerException
    at ru.ispras.fortress.data.types.bitvector.BitVector.notNullCheck(BitVector.java:772)
    at ru.ispras.fortress.data.types.bitvector.BitVector.valueOf(BitVector.java:535)
    at ru.ispras.verilog.parser.model.basis.Literal.getBitVector(Literal.java:222)
    at ru.ispras.verilog.parser.model.basis.Literal.getValue(Literal.java:356)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_primary(VerilogTreeBuilder.java:729
6)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_expression(VerilogTreeBuilder.java:
7146)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_task_statement(VerilogTreeBuilder.j
ava:5031)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_statement(VerilogTreeBuilder.java:4
633)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_block_statement(VerilogTreeBuilder.
java:6057)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_statement(VerilogTreeBuilder.java:4
737)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_process(VerilogTreeBuilder.java:360
0)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_item(VerilogTreeBuilder.java:958)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_module(VerilogTreeBuilder.java:634)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.ast_root(VerilogTreeBuilder.java:440)
    at ru.ispras.verilog.parser.grammar.VerilogTreeBuilder.startRule(VerilogTreeBuilder.java:382)
    at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:216)
    at ru.ispras.verilog.parser.VerilogFrontend.startBuilder(VerilogFrontend.java:220)
    at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:231)
    at ru.ispras.verilog.parser.VerilogFrontend.start(VerilogFrontend.java:235)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:120)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:46)
```

History

#1 - 10/16/2015 02:35 PM - Sergey Smolov

This error also appears on src/test/verilog/ram/ram_testbench.v

#2 - 10/21/2015 06:28 AM - Alexander Kamkin

- Status changed from New to Resolved

#3 - 10/21/2015 04:50 PM - Sergey Smolov

- Status changed from Resolved to Verified

#4 - 03/01/2018 02:41 PM - Alexander Kamkin

- Status changed from Verified to Closed