Retrascope - Task #5872

HDL file meta info

04/22/2015 11:37 AM - Sergey Smolov

Status:	Closed	**Start date:**	04/22/2015
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:	Engine (Parser)	**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	20150701

Description

Keep HDL file name at top-level module meta-information.

History

#1 - 04/22/2015 11:37 AM - Sergey Smolov

- Category set to 127

#2 - 04/23/2015 03:39 PM - Sergey Smolov

- Status changed from New to Open

#3 - 04/23/2015 05:26 PM - Sergey Smolov

- % Done changed from 0 to 50

I've implemented this for VHDL.

The Verilog parser will be improved soon.

#4 - 04/24/2015 05:13 PM - Sergey Smolov

- Status changed from Open to Resolved

- % Done changed from 50 to 100

Done for VHDL.

#5 - 07/01/2015 10:36 AM - Sergey Smolov

- Status changed from Resolved to Verified

#6 - 07/01/2015 11:49 AM - Sergey Smolov

- Status changed from Verified to Closed

- Published in build set to 20150701