Retrascope - Task #5588

extend HDL test suite

01/28/2015 12:47 PM - Sergey Smolov

Status:	Verified	**Start date:**	01/28/2015
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:	Test Suite	**Estimated time:**	0.00 hour
Target version:	1.0		
Detected in build:	master	**Published in build:**	

Description

Extend a set of HDL (Verilog. VHDL) designs that are used as project test suite.

The collection of open-source benchmarks is available here: http://ddd.fit.cvut.cz/prj/Benchmarks/

History

#1 - 03/13/2015 03:07 PM - Sergey Smolov

- Subject changed from [project] extend HDL test suite to extend HDL test suite

- Category set to Test Suite

#2 - 03/13/2015 04:01 PM - Sergey Smolov

Check samples of asynchronous Verilog designs here: async.org.uk

Keywords: Tech report towards asynchronous power management

#3 - 03/19/2015 07:30 PM - Sergey Smolov

Look at synthagate examples coming with Decider.

#4 - 03/11/2016 04:21 PM - Sergey Smolov

- Target version changed from 0.1 to 0.2

#5 - 10/25/2016 12:27 PM - Sergey Smolov

- Detected in build changed from svn to master

#6 - 09/12/2017 03:32 PM - Sergey Smolov

- Target version changed from 0.2 to 1.0

#7 - 09/28/2017 04:24 PM - Sergey Smolov

- Status changed from New to Resolved

- % Done changed from 0 to 100

ITC99 designs are added in ab8526a7.
Some perspective benchmarks are stored in the internal sub-project.

#8 - 09/28/2017 04:24 PM - Sergey Smolov

- Status changed from Resolved to Verified