Retrascope - Task #5549

[vhdl][cfg][parser] add support of instantiation

01/12/2015 03:56 PM - Sergey Smolov

Status:	Closed	**Start date:**	01/12/2015
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.2		
Detected in build:	svn	**Published in build:**	20150307

Description

Implement a support in modules' instances at the CFG level.
Elaborate VHDL/Verilog designs from project test suite, that contain instances.

History

#1 - 01/21/2015 12:35 PM - Sergey Smolov

- Status changed from New to Open

#2 - 01/22/2015 12:04 PM - Sergey Smolov

- Subject changed from [cfg] add support of instantiation to [vhdl][cfg][parser] add support of instantiation

#3 - 02/02/2015 03:31 PM - Sergey Smolov

- Status changed from Open to Resolved

- % Done changed from 0 to 100

- Published in build set to r1509

#4 - 03/07/2015 11:08 PM - Sergey Smolov

- Status changed from Resolved to Closed

- Published in build changed from r1509 to 20150307