Verilog Translator - Bug #5164

После директивы `endif в той же строчке могут идти лексемы

07/29/2014 06:31 AM - Alexander Kamkin

Status:	Closed	**Start date:**	07/29/2014
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	
Platform:			

Description

В частности допустим следующий код:

```
x = (`ifdef X
       1
     `else
       2
     `endif);
```

History

#1 - 07/29/2014 06:42 AM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 08/20/2014 02:13 PM - Alexander Kamkin

- Status changed from Resolved to Closed