Verilog Translator - Task #5160

Обработка комментариев в define

07/28/2014 03:04 PM - Alexander Kamkin

Status:	Closed	**Start date:**	07/28/2014
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	

Description

Verilog-препроцессор (в отличие от препроцессора C) игнорирует комментарии.

```
`define my_constant my_value // my_comment: my_constant = my_value
```

Нужно это учесть.

History

#1 - 07/28/2014 07:36 PM - Alexander Kamkin

- Status changed from New to Resolved

#2 - 08/20/2014 02:13 PM - Alexander Kamkin

- Status changed from Resolved to Closed