Verilog Translator - Task #5092

Merging declaration parts for the same variable

07/16/2014 02:59 PM - Alexander Kamkin

Status:	Closed	**Start date:**	07/16/2014
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	

Description

Translator should perform preprocessing of the AST merging declaration parts for the same variable:

```
output x;
reg x;

=> output/reg x;
```

History

#1 - 07/21/2014 10:11 AM - Alexander Kamkin

- Status changed from New to Resolved

Set<Declaration> Declaration.getNamesakes() - получение множества деклараций.

#2 - 08/01/2014 11:20 AM - Alexander Kamkin

- Status changed from Resolved to Closed