# Verilog Translator - Task #4408

## Scope.YES & Scope.NO

07/29/2013 07:55 PM - Alexander Kamkin

| | | | |
|---|---|---|---|
| **Status:** | Closed | **Start date:** | 07/29/2013 |
| **Priority:** | Normal | **Due date:** | |
| **Assignee:** | Alexander Kamkin | **% Done:** | 0% |
| **Category:** | | **Estimated time:** | 0.00 hour |
| **Target version:** | 0.1 | | |
| **Detected in build:** | svn | **Published in build:** | |

**Description**

There is no difference.

### History

**#1 - 04/29/2014 01:55 PM - Alexander Kamkin**

*- Target version set to 0.1*

**#2 - 08/24/2018 12:45 PM - Alexander Kamkin**

*- Status changed from New to Resolved*

**#3 - 08/24/2018 12:57 PM - Alexander Kamkin**

*- Status changed from Resolved to Closed*