Verilog Translator - Task #4126

Unification of AST_EDGE and AST_TABLE_EDGE

04/19/2013 09:45 AM - Alexander Kamkin

Status:	New	**Start date:**	04/19/2013
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	

Description

If there is a similarity between ast_edge and ast_table_edge, the nodes may be unified.

History

#1 - 04/29/2014 01:57 PM - Alexander Kamkin

- Target version set to 0.1