Verilog Translator - Task #4123

Support for system timing check

04/18/2013 10:50 AM - Alexander Kamkin

Status:	Closed	**Start date:**	04/18/2013
Priority:	Low	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.3		
Detected in build:	svn	**Published in build:**	

Description

Grammar + AST.

History

#1 - 04/18/2013 10:58 AM - Alexander Kamkin

- Subject changed from Support for system timing check. to Support for system timing check

#2 - 04/29/2014 01:57 PM - Alexander Kamkin

- Target version set to 0.1

#3 - 04/29/2014 01:58 PM - Alexander Kamkin

- Target version changed from 0.1 to 0.3

#4 - 08/31/2018 12:30 PM - Alexander Kamkin

- Status changed from New to Resolved

Grammar has been written, but descriptions are ignored.

#5 - 08/31/2018 02:17 PM - Alexander Kamkin

- Status changed from Resolved to Closed