Verilog Translator - Task #3514

Поддержка в препроцессоре define с параметрами

09/28/2012 08:57 AM - Alexander Kamkin

Status:	Rejected	**Start date:**	09/28/2012
Priority:	Low	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	svn	**Published in build:**	

Description

`define(x, y) (x) + (y)

History

#1 - 04/29/2014 01:58 PM - Alexander Kamkin

- Target version set to 0.1

#2 - 09/06/2018 12:36 PM - Alexander Kamkin

- Status changed from New to Rejected

Duplicated issue.