Verilog Translator - Bug #10505

ERROR: [Internal] 11 must be within range [0, 1)

09/30/2020 01:51 PM - Sergey Smolov

Status:	New	**Start date:**	09/30/2020
Priority:	Normal	**Due date:**	
Assignee:	Alexander Kamkin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	git	**Published in build:**	
Platform:			

Description

```
java.lang.IndexOutOfBoundsException: 11 must be within range [0, 1)
    at ru.ispras.fortress.util.InvariantChecks.checkBounds(InvariantChecks.java:190)
    at ru.ispras.fortress.data.types.bitvector.BitVector.field(BitVector.java:309)
    at ru.ispras.verilog.parser.interpreter.VerilogOperations$34.calculate(VerilogOperations.java:
745)
    at ru.ispras.fortress.calculator.OperationGroup.calculate(OperationGroup.java:141)
    at ru.ispras.fortress.transformer.Reducer$OperationRule.apply(Reducer.java:147)
    at ru.ispras.fortress.transformer.NodeTransformer.applyRule(NodeTransformer.java:173)
    at ru.ispras.fortress.transformer.NodeTransformer.updateNode(NodeTransformer.java:183)
    at ru.ispras.fortress.transformer.NodeTransformer.onOperationEnd(NodeTransformer.java:231)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitOperation(ExprTreeWalker.java:173)
    at ru.ispras.fortress.expression.ExprTreeWalker.visitNode(ExprTreeWalker.java:123)
    at ru.ispras.fortress.expression.ExprTreeWalker.visit(ExprTreeWalker.java:93)
    at ru.ispras.fortress.transformer.NodeTransformer.walk(NodeTransformer.java:54)
    at ru.ispras.fortress.transformer.Reducer.reduce(Reducer.java:183)
    at ru.ispras.fortress.transformer.Reducer.reduce(Reducer.java:248)
    at ru.ispras.verilog.parser.interpreter.VerilogCalculator.reduce(VerilogCalculator.java:50)
    at ru.ispras.verilog.parser.transformer.VerilogTransformerOperation.transform(VerilogTransform
erOperation.java:66)
    at ru.ispras.verilog.parser.transformer.VerilogTransformerComposite.transform(VerilogTransform
erComposite.java:57)
    at ru.ispras.verilog.parser.transformer.VerilogTransformer.transform(VerilogTransformer.java:2
14)
    at ru.ispras.verilog.parser.transformer.VerilogTransformer.transform(VerilogTransformer.java:2
26)
    at ru.ispras.verilog.parser.transformer.VerilogTransformer.transform(VerilogTransformer.java:2
45)
    at ru.ispras.verilog.parser.transformer.VerilogTransformer.onAssignStatementBegin(VerilogTrans
former.java:84)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor$3.onBegin(VerilogNodeVisitor.java:285)
    at ru.ispras.verilog.parser.walker.VerilogNodeVisitor.onBegin(VerilogNodeVisitor.java:770)
    at ru.ispras.verilog.parser.core.TreeWalker.onBegin(TreeWalker.java:102)
    at ru.ispras.verilog.parser.core.TreeWalker.start(TreeWalker.java:81)
    at ru.ispras.verilog.parser.transformer.VerilogTransformer.run(VerilogTransformer.java:55)
    at ru.ispras.verilog.parser.elaborator.VerilogInstantiator.instantiate(VerilogInstantiator.jav
a:198)
    at ru.ispras.verilog.parser.elaborator.VerilogInstantiator.instantiateProcess(VerilogInstantia
tor.java:144)
    at ru.ispras.verilog.parser.elaborator.VerilogDesign$1$1.next(VerilogDesign.java:212)
    at ru.ispras.verilog.parser.elaborator.VerilogDesign$1$1.next(VerilogDesign.java:199)
    at ru.ispras.verilog.parser.backends.design.typecast.VerilogTypeCaster.start(VerilogTypeCaster
.java:43)
    at ru.ispras.verilog.parser.VerilogDesignBackends.start(VerilogDesignBackends.java:55)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:219)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.util.VerilogBenchmarkTest.runTest(VerilogBenchmarkTest.java:62)
    at ru.ispras.verilog.parser.VerilogIwlsTestSuite.runTest_opencores_pci_target_unit(VerilogIwls
TestSuite.java:3941)
```

Associated revisions

Revision e023b828 - 09/30/2020 01:51 PM - Sergey Smolov

junit: uncomment tests that fall because of #10505

Signed-off-by: Sergey Smolov <smolov@ispras.ru>

History

#1 - 09/30/2020 01:52 PM - Sergey Smolov

To reproduce the bug is to switch to **bug10505** branch and run the following test suites:

ru.ispras.verilog.parser.VerilogQuipTestSuite
ru.ispras.verilog.parser.VerilogIwlsTestSuite