# Verilog Translator - Bug #10382

## java.lang.IllegalArgumentException: expression=(BVREPEAT test.uut._saxi_maskwidth 1)

06/18/2020 09:07 AM - Sergey Smolov

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|---|---|---|---|
| **Status:** | Closed | **Start date:** | 06/18/2020 |
| **Priority:** | Normal | **Due date:** | |
| **Assignee:** | Sergey Smolov | **% Done:** | 100% |
| **Category:** | | **Estimated time:** | 0.00 hour |
| **Target version:** | 0.1 | | |
| **Detected in build:** | git | **Published in build:** | 0.1.3-beta-201002 |
| **Platform:** | | | |

**Description**

```
java.lang.IllegalArgumentException: expression=(BVREPEAT test.uut._saxi_maskwidth 1)
    at ru.ispras.fortress.util.InvariantChecks.checkTrue(InvariantChecks.java:53)
    at ru.ispras.fortress.util.InvariantChecks.checkNotNull(InvariantChecks.java:109)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.defineParameter(VerilogElaborator.jav
a:1074)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createVariableAndBinding(VerilogElabo
rator.java:526)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createVariablesAndBindings(VerilogEla
borator.java:910)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createVariablesAndBindings(VerilogEla
borator.java:883)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.expand(VerilogElaborator.java:330)
    at ru.ispras.verilog.parser.elaborator.VerilogElaborator.start(VerilogElaborator.java:231)
    at ru.ispras.verilog.parser.VerilogSyntaxBackends.start(VerilogSyntaxBackends.java:55)
    at ru.ispras.verilog.parser.VerilogTranslator.start(VerilogTranslator.java:212)
    at ru.ispras.verilog.parser.sample.VerilogPrinter.main(VerilogPrinter.java:45)
    at ru.ispras.verilog.parser.sample.VerilogPrinterTestCase.runTest(VerilogPrinterTestCase.java:
50)
```

### Associated revisions

**Revision ff8ec5fa - 06/18/2020 09:09 AM - Sergey Smolov**

test: jUnit test case (#10382)

Signed-off-by: Sergey Smolov <smolov@ispras.ru>

**Revision cd3bd605 - 06/22/2020 01:04 PM - Sergey Smolov**

bugfix (#10382)

Add rule for BVEXTRACT operation.

Signed-off-by: Sergey Smolov <smolov@ispras.ru>

### History

**#1 - 06/18/2020 09:09 AM - Sergey Smolov**

Run **ru.ispras.verilog.parser.sample.Bug10382TestCase** to reproduce the bug.

**#2 - 06/22/2020 01:06 PM - Sergey Smolov**

*- % Done changed from 0 to 100*

*- Assignee set to Sergey Smolov*

*- Status changed from New to Resolved*

**#3 - 10/02/2020 02:53 PM - Sergey Smolov**

*- Published in build set to 0.1.3-beta-201002*

*- Status changed from Resolved to Closed*